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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,326	07/03/2003	Daniel M. Kinzer	IR-2541 DIV	4283

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/613,326	KINZER ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,8-10,12,14-17,19 and 27-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,8-10,12,14-17,19 and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 3-4, 8-10, 12, 14-17, 19 and 27-29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the drawings and there is no adequate description in the disclosure for the claimed limitations of a current path from said source electrode to said drain electrode includes a vertical component, as recited in claims 1 and 12.

There is no support in the specification for first and second laterally spaced and metallized layers each connected to one of said P region and said N region, as recited in claims 1 and 12.

There is no support in the drawings and there is no adequate description in the disclosure for the claimed limitations of first, second metallized layers comprising source and drain electrodes respectively, wherein the current path from said first conductive electrode to said second conductive electrode having a vertical component, as recited in claim 27.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3-4, 8-10, 12, 14-17, 19 and 27-29 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claimed limitations of first, second and third metallized layers comprising source, drain and gate electrodes respectively, wherein a current path from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface, as recited in claims 1 and 12, and first and second metallized layers comprising source and drain electrodes respectively, wherein the current path from said first conductive electrode to said second conductive electrode having a vertical component which is generally perpendicular to said first surface, as recited in claim 27, are unclear as to how the respective electrodes can be formed on one first major surface, and at the same time have a vertical component which is generally perpendicular to said first major surface.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-4, 8-10, 12, 14-17, 19 and 27-29, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa et al. (5,105,243) in view of Coe et al. (5,128,730) and Rinne et al. (6,117,299).

Regarding claims 1, 12, 14 and 27, Nakagawa et al. teach in figure 2 and related text a semiconductor device comprising a silicon wafer having parallel first and second major surfaces; at least one P region 16 and at least one N region 10 in the wafer which meet at a PN junction within the silicon wafer; first 24 and second 26 laterally spaced and electrode layers formed on the first major surface and each connected to one of said P region and said N region; a bottom electrode layer 14 extending across the second major surface; and

a third electrode layer 22 atop the first major surface which is laterally spaced from the first and second layers; the first, second and third layers comprising source, drain and gate electrodes respectively of a MOS gated device,

wherein a current path inside said silicon wafer from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface (since Nakagawa et al. teach an electrode 14 located on the second major surface of the device).

Nakagawa et al. do not teach using the device in a flip chip arrangement, wherein the electrodes comprise metal.

Coe et al. teach electrodes comprise metal.

Rinne et al. teach in figure 3 and related text a flip chip.

It would have been obvious to one having ordinary skill in the art at the time the invention was made use Nakagawa et al.'s device in a flip chip arrangement, wherein the electrodes comprise metal, in order to use the device in an application which requires flip chip and in order to improve the conductivity of the device by using conventional material, respectively.

Regarding claims 27 and 28, Nakagawa et al. teach in figures 6-8 and related text a high conductivity element sinker located outside said region of one conductivity type and has higher conductivity than said body region.

Regarding claims 12 and 3, 4, 9-10, 16, Rinne et al. teach in figure 3 and related text a plurality of contact bumps connected to each of said first and second metallized layers; said plurality of contact bumps connected to said first metallized layer being aligned along a first straight row; said plurality of contact bumps connected to the second metallized layer being aligned along a second straight row parallel to the first straight row.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to connect each of said first and second metallized layers in Nakagawa et al.'s device to a plurality of contact bumps wherein said plurality of contact bumps connected to said first metallized layer being aligned along a first straight row, and said plurality of contact bumps connected to the second metallized layer being aligned along a second straight row parallel to the first straight row, in order to operate

the device in its intended use by providing economical external connections to the device.

Regarding claims 8 and 15, prior art does not state that the bottom metallized layer is substantially thicker than all of the first and second metallized layers.
It would have been obvious to one having ordinary skill in the art at the time the invention was made for the bottom metallized layer is substantially thicker than all of the first and second metallized layers, in order to improve the thermal conduction of the device. It has been held that discovering an optimum value of a result effective variable of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPA 215 (CCPA 1980).

Regarding claims 17 and 19, Nakagawa et al. teach in figure 2 and related text a silicon wafer is a rectangular wafer having an area defined by a given length and a given width, the length being greater than the width. Prior art's device comprises said first and second rows of bumps being parallel to one another and being symmetric about a diagonal line across the wafer.

Regarding claim 29, Nakagawa et al. do not teach said high conductivity element is a metallic material residing in a trench formed in said body of said die.
It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a high conductivity element being a metallic material

residing in a trench formed in said body of said die in Nakagawa et al.'s device in order to have better control over conductivity and the electrical characteristics of the high conductivity element.

Response to Arguments

Applicant argues that there is support in the specification at page 7, lines 7-13 for "current path that includes vertical portions", as recited in claims 1, 12 and 27.

The examiner agrees that a vertical device can have vertical current path. However, there is no support in the specification for the claimed limitations of a current path from said source electrode to said drain electrode includes a vertical component, as recited in claims 1 and 12, and there is no support in the sepcification for the claimed limitations of first, second metallized layers comprising source and drain electrodes respectively, wherein the current path from said first conductive electrode to said second conductive electrode having a vertical component, as recited in claim 27, because said source electrode and said drain electrode are located on one major surface and above each other.

Applicant argues that Nakagawa et al. do not teach that a current path inside said silicon wafer from said source electrode to said drain electrode includes a vertical component which is generally perpendicular to said first major surface, because the

source and drain electrodes in Nakagawa et al.'s device are located on the same surface.

Applicant's device comprises source and drain electrodes located on the same surface. If the source and drain electrodes in applicant's device can create a current path having a vertical component which is generally perpendicular to said first major surface from said source electrode to said drain electrode, so can said source electrode and said drain electrode in Nakagawa et al.'s device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
3/28/2008

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